Abstract

The present invention relates to a method of coupling at
least one (conventional) unit processing data in a sequen-
5 tial manner, e.g. a CPU, von-Neumann-Processor and/or micro-
controller, the (conventional) unit for data processing com-
prising an instruction pipeline, and an array for processing
data comprising a plurality of data processing cells, e.g. a
preferably coarse grain and/or preferably runtime reconfigu-
10 rable data processor, FPGA, DFP, DSP, XPP or chaemeleon-tech-
nology-like data processing fabric, wherein the array is cou-
pled to the instruction pipeline.

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